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EXAMINER	
COSIMANO, EDWARD R	
ART UNIT	PAPER NUMBER
2863	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,751	ABERLE ET AL.	
	Examiner	Art Unit	
	Edward R. Cosimano	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The Oath/Declaration filed 20 March 2006 in view of the application data sheet filed 22 March 2005 and the Abstract as originally filed are acceptable to the examiner.

2. Applicant's claim for the benefit of an earlier filing date pursuant to 35 U.S.C. sections 120 and 371 is acknowledged.

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

4. The examiner has considered the prior art cited in the base applications.

5. The drawing filed on 22 March 2005 is objected to because:

A) there is only one figure in the drawings of the instant application applicant's designation of this figure as "Fig. 1" in the drawing is improper pursuant to 37 CFR 1.84(u)(1), and therefore this legend must be removed.

B) the drawing fails to comply with 37 CFR 1.84(n,o) because it contains unlabeled depiction of a feature of the invention that is not readily recognizable from the depicted symbol. Therefore applicant is required to provide suitable descriptive title legend for the feature of the invention designated by reference number 60 in the figure which applicant has described by using the phrase "selection unit 60" in the disclosure located in the paragraphs between page 6, line 24, and page 7, line 30, "The circuit configuration ... a selection unit 60. The ... selection unit 60 ... selection unit 60 ... selection unit 60 ... selection unit 60 ... DC voltage there must be an error present.";

C) the drawing fails to comply with 37 CFR 1.84(p)(5) because it does not include the following reference legend mentioned in the description, note reference legend 20 which has been mentioned in the written description of the figure located between page 6, line 24, and page 7, line 9, "The circuit configuration ... partial systems 20. Provided in the partial systems 20a, 20b and 20c is ... with a voltage measuring device 22.", and see also in regard to the corresponding objection to the disclosure.

D) The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the:

(1) the actions and conclusions that would be drawn from performing the process recited as claims 12-17, that can not be depicted by a circuit that may function as recited in these claims,

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5.1 Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The disclosure is objected to because of the following informalities:

A) because claims 1-17 as filed may either (1) be cancelled during the prosecution of the instant application, or (2) appear as differently numbered claims in any patent that may mature from the instant application, then applicant's reference to these claims in the disclosure between page 2, line 3, and page 6, line 17, "The invention solves this ... switching state of the second switching means.", will cause potential confusion. In this regard note the proposed amendments to these paragraphs below.

B) because there is only one figure in the drawings of the instant application applicant's designation of this figure as "Fig. 1" in the paragraphs of the disclosure located between page 6, line 24, and page 7, line 9, is improper pursuant to 37 CFR 1.84(u)(1) and in view of 37 CFR 1.74, and therefore the references to "Fig. 1" must be removed. In this regard note the proposed amendments to these paragraphs below.

C) errors and/or inconsistencies between the drawing filed on 22 March 2005 and the written description have been noted:

(1) if applicant chooses not to add reference legend 20 to the figure, note above, then the specification fails to comply with 37 CFR 1.84(p)(5) because the specification includes an explicit reference to this reference legend in the description of the figure located between page 6, line 24, and page 7, line 9, "The circuit configuration ... partial systems 20. Provided in the partial systems 20a, 20b and 20c is ... with a voltage measuring device 22.". In this regard it is noted that the figure depicts "partial systems 20a, 20b and 20c" and the disclosure, with the above exception consistently references this feature of the invention as "partial systems 20a, 20b and 20c" in the paragraph located between page 6, line 24, and page 8, line 12, "The circuit configuration ... a criterion for the presence of a short-circuit.". It is therefore suggested that the paragraph located between page 6, line 24, and page 7, line 9, should be amended as follows, change the reference to "partial systems 20" to reference --partial systems 20a, 20b and 20c--, note the proposed amendment below.

D) the disclosure lacks a statement of –We claim:--, as required by Office policy as set forth in MPEP 608.01(m).

E) in view of the above objections it is suggested that the following paragraphs be amended as indicated:

(1) at page 2, lines 3-4:

The invention solves this problem by providing a circuit configuration with the features of ~~claim 1~~ the claimed machine and a method with the features of ~~claim 12~~ the claimed process.

(2) at page 2, lines 23-25:

In a further development of the invention, ~~according to claim 2~~ a first impedance is switched parallel to the first switching means and a second impedance is switched parallel to the second switching means.

(3) at page 3, lines 26-29:

In a further development of the invention, ~~according to claim 3~~ the first voltage connection is a supply voltage connection for the partial systems. This simplifies the

circuit configuration and the circuit design, as no further voltages have to be provided, for example with the aid of separate voltage regulators.

(4) at page 4, lines 1-4:

In a further development of the invention, ~~according to claim 4~~ the second voltage connection is the ground connection. This likewise simplifies the circuit configuration and the circuit design, as the ground voltage or the ground potential is available to all partial systems as general reference voltage or reference potential.

(5) at page 4, lines 5-7:

In a further development of the invention, ~~according to claim 5 or 6~~ the first or second switching means is a transistor. Transistors, for example bipolar transistors or MOS transistors, have good switching properties, are available and cheap to acquire.

(6) at page 4, lines 8-13:

In a further development of the invention, ~~according to claim 7~~ the first and the second transistor are transistors complementary to one another. Examples of complementary transistors are bipolar npn-type or pnp-type transistors or n-type or p-type MOS transistors. Because the transistors are complementary to one another, a complementary switching pattern can be achieved with the aid of a common selection signal, i.e. only one of the two transistors is conductive in each case.

(7) at page 4, lines 14-16:

In a further development of the invention, ~~according to claim 8~~ the first and second impedance are ohmic resistors. Ohmic resistors are cheap and dimensioning of the circuit configuration is simple to perform.

(8) at page 4, lines 17-20:

In a further development of the invention, ~~according to claim 9~~ the partial systems are connected to the signal line loop with high resistivity. This enables any number of partial systems to be connected to the signal line loop. Dimensioning depending on the number is not necessary.

(9) at page 4, lines 21-23:

In a further development of the invention, ~~according to claim 10~~ the signal line loop is looped through the partial systems. Each partial system can influence the state of

the signal line loop, for example interrupt the signal line loop, depending on its internal operating state.

(10) at page 4, lines 24-28:

In a further development of the invention, ~~according to claim 11~~ the partial systems have means for interrupting the signal line loop depending on their functional state. If, for example, an internal error occurs in a partial system, the corresponding partial system may cause an internal interruption of the signal line loop. This interruption can be detected by all the other partial systems and may lead to triggering of appropriate error recovery.

(11) at page 5, lines 1-13:

The method ~~according to claim 12~~ for identifying error situations of an electrical signal line loop with several partial systems connected thereto, in particular partial systems for voltage generation in a fuel cell system, comprises the steps: charging a first end of the signal line loop with a first voltage of a first voltage connection and connecting a second end of the signal line loop to a second voltage connection via a second impedance, alternating with this, connecting the first end to the first voltage connection via a first impedance and charging the second end with the second voltage of the second voltage connection, and measuring and evaluating the signal course on the signal line loop to identify the error situation. The error situations comprise one or more interruptions of the signal line loop and short-circuits of the signal line loop against a voltage. In the method according to the invention the ends of the signal line loop are alternately charged with different voltages. In the case of error-free operation this gives rise to an alternating voltage signal which is evaluated by the partial systems connected to the signal line loop.

(12) at page 5, lines 14-19:

In a further development of the method ~~according to claim 13~~, during evaluation of the signal course is detected which partial systems constantly measure the first voltage, which partial systems measure an undefined voltage and which partial systems constantly measure the second voltage and short-circuits or short-circuits to ground and/or

interruptions of the signal line loop are ascertained and/or located as a function of the voltages measured by the individual partial systems.

(13) at page 5, lines 20-24:

In a further development of the method ~~according to claim 14~~, during evaluation of the signal course an error is identified if at least one partial system measures a DC voltage. Without an interruption or short-circuit of the signal line loop the voltage of the signal line loop alternates between two voltage levels. If a DC voltage is measured, consequently there must be an error present in the form of an interruption or a short-circuit.

(14) at page 5, lines 25-32:

In a further development of the method ~~according to claim 15~~, during evaluation of the signal course a short-circuit of the signal line loop with the first voltage connection is identified if all the partial systems measure a DC voltage with the level of the first voltage. If the signal line loop is short-circuited with the first voltage connection, the first voltage is continuously applied to the signal line loop. This can consequently be drawn on as a criterion for a short- circuit of the signal line loop with the first voltage connection. Any overload currents caused by the short-circuit which occasion a response from safety devices or failure of the overall system are not taken into account in this.

(15) at page 6, lines 1-5:

In a further development of the method ~~according to claim 16~~, during evaluation of the signal course a short-circuit of the signal line loop with the second voltage connection is identified if all the partial systems measure a DC voltage with the level of the second voltage. If the signal line loop is short-circuited with the second voltage connection the second voltage is continuously applied to the signal line loop.

(16) at page 6, lines 6-17:

In a further development of the method ~~according to claim 17~~, during evaluation of the signal course an interruption at a location on the signal line loop is identified if partial systems on one side of the location constantly measure the first voltage and partial systems on the other side of the location constantly measure the second voltage. If there is an interruption of the signal line loop, the first voltage is continuously applied to the

part of the signal line loop facing the first switching means, irrespective of the switching state of the first switching means. Either this part of the signal line loop is charged with the first voltage with the aid of the switching means or it is connected to the first voltage connection via the first impedance. As this part of the signal line loop is in a highly resistive state, the first voltage applies in both cases. The situation is analogous for the part of the signal line loop facing the second switching means. The second voltage is continuously applied to it, irrespective of the switching state of the second switching means.

(17) at page 6, lines 21-23:

~~Fig. 1, as~~ The single figure, shows a schematic block diagram of a circuit configuration for identifying error situations in interconnected partial systems for voltage generation in a fuel cell system.

(18) between page 6, line 24, and page 7, line 9:

The circuit configuration ~~of Fig. 1~~ shown in the single figure comprises an electrical signal line loop 10 with a first end 11 and a second end 12, three partial systems 20a, 20b and 20c, connected thereto and serving, for example, to generate high voltages in the fuel cell system, a voltage source with a first voltage connection 30 for providing a first voltage, a first pnp-type transistor 40, a second npn-type transistor 41, complementary to the first transistor 40, a first resistor 50, a second resistor 51 and a selection unit 60. The collector-emitter section of the first transistor 40 is looped in parallel to the resistor 50 between the first end 11 of the signal line loop 10 and the voltage connection 30. The collector-emitter section of the second transistor 41 is looped in parallel to the second resistor 51 between the second end 12 of the signal line loop 10 and a ground contact 31. The selection unit 60 is connected to the respective basic connections of the transistors 40 and 41. The signal line loop 10 is looped through the partial systems ~~20~~ 20a, 20b and 20c. Provided in the partial systems 20a, 20b and 20c is in each case a relay 21 for interrupting the signal line loop depending on the functional state of the respective partial system. The partial systems 20a, 20b and 20c are in each case connected with high resistivity to the signal line loop 10 and in each case determine the voltage on the signal line loop with a voltage measuring device 22.

6.1 Appropriate correction is required.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7.1 Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7.1.1 In regard to claim 1, it is noted that this claim recites a "Circuit configuration" with the function of "identifying error situations in interconnected partial systems for voltage generation in a fuel cell system", where the circuit configuration includes the structures of a "selection unit", at least one "partial system" and an "electrical signal line loop" that is formed by serially interconnecting a first voltage source to a first selectable/controllable switch and then to one or more "serially/parallelly interconnected partial systems" and then to a second selectable/controllable switch and then to a second voltage source or ground. Where the "selection unit" functions to select either the first switch or the second switch, and the "partial systems" function to evaluate the state of the signal line.

7.1.2 From the circuit that is described in claim 1, one of ordinary skill at the time the invention was made would interpret the circuit of claim 1 to operate in such that the circuit formed by the combined structures of the first voltage source, the first switch, the one or more partial systems, the second switch and the second voltage source will ONLY BE INTERCONNECTED TO FORM A COMPLETE AND OPERATIVE ELECTRICAL CIRCUIT when both the first switch and the second switch have been turned "ON" that is conductive so that that power/current may flow from the first voltage source to the second voltage source by flowing through the first switch, the one or more partial systems and the second switch. In view of the recognized operation of the "circuit configuration" that is described in claim 1 is contrary to the disclosed alternative selection of the first switch or second switch by the selection unit, see the paragraph located at page 7, lines 10-25, "The selection unit 60 ... forward voltage of the transistor 41.", then one of ordinary skill at the time the invention was made would be confused by how the claimed "circuit configuration" would function TO IDENTIFY ERROR SITUATIONS IN INTERCONNECTED PARTIAL SYSTEMS when the first switch or the

second switch is alternatively selected to be conductive and hence A COMPLETE AND OPERATIVE ELECTRICAL CIRCUIT WILL NOT BE FORMED.

7.1.3 It is further noted that one of ordinary skill at the time the invention was made would be confused by how claims 1-11 THAT POSITIVELY RECITE THE EVALUATION OF THE STATE OF THE SIGNAL LOOP, BUT FAIL POSITIVELY RECITE THE "IDENTIFICATION OF AN ERROR SITUATION IN AN INTERCONNECTED PARTIAL SYSTEM" would function to achieve the identification of an error in a partial system. This confusion occurs because one of ordinary skill at the time the invention was made would recognize that the recited circuit of the "circuit configuration" does not function to achieve the recited purpose or function of "identifying error situations in interconnected partial systems", since the claimed circuit configuration does not determine if an "error situation in the interconnected partial systems" has occurred.

7.1.4 To the structure recited in claim 1 it is noted that claim 2 ads the additional structure that a first resistor is connected in parallel across the first switch and a second resistor is connected in parallel across the second switch. Based on the additional structure of claim 2, one of ordinary skill at the time the invention was made would interpret the circuit configuration of claim 2 to ALWAYS BE INTERCONNECTED TO FORM A COMPLETE AND OPERATIVE ELECTRICAL CIRCUIT between the first voltage source and the second voltage source REGARDLESS of whether or not the operating state of either the first switch or the second switch has been turned "ON" that is conductive. There will always be a conductive path for power/current to flow from the first voltage source to the second voltage source because the power/current will flow through the path of least resistance, that is:

A) if the first switch is ON or conductive then power will flow through the first switch, otherwise when the first switch is OFF or nonconductive, then power will flow through the first resistor; and

B) if the second switch is ON or conductive then power will flow through the second switch, otherwise when the second switch is OFF or nonconductive, then power will flow through the second resistor.

In view of the recognized operation of the "circuit configuration" that is described in claim 2 is contrary to the disclosed alternative selection of the first switch or second switch by the selection

unit, see the paragraph located at page 7, lines 10-25, "The selection unit 60 ... forward voltage of the transistor 41.", then one of ordinary skill at the time the invention was made would be confused by how the claimed "circuit configuration" would function TO IDENTIFY ERROR SITUATIONS IN INTERCONNECTED PARTIAL SYSTEMS by alternatively selecting the first switch or the second switch to be conductive and A COMPLETE AND OPERATIVE ELECTRICAL CIRCUIT IS ALWAYS FORMED.

7.2 In regard to claim 11, one of ordinary skill at the time the invention was made would be confused by how the claimed partial systems of the claimed "circuit configuration" would function TO INTERRUPT THE SIGNAL LINE LOOP BASED ON THE FUNCTION [[STAGE]] STATE because, the functional state of the "partial system" is not positively recited as being determined and hence could not be used to interrupt the signal line loop.

7.2.1 Further in regard to claim 11, applicant's use of the word "stage" at line 4 of claim 11 is confusing because it is unclear how the recited "partial system" could have a stage. In view of this it is noted that the word "stage" should be –state--.

7.3 In regard to claims 12-17, as one of ordinary skill at the time the invention was made would interpret these claims the actions of charging the signal line loop with a voltage would produce a "short-circuit" condition in the signal line loop where both ends of the signal line loop are at the same potential. Hence, one of ordinary skill at the time the invention was made would be confused because it unclear how the action of charging the signal line loop from one end and then from the other end would produce any measurement data/information that could be evaluated to provide a useful and beneficial indication of en "error situation in an electrical signal line loop". It is noted that this same problem may occur in claims 1-11, if applicant amends claim 1 to recite similar subject matter to claim 12.

7.4 Claims not explicitly mentioned above include the above noted defect(s) because the unmentioned claims are depend either directly or indirectly from one or more of the above noted claim(s).

8. The examiner has cited prior art of interest, for example:

A) Summers et al (3,808,534) or Jamoua et al (5,063,534) or Zydek et al (WO 96/38736 or 5,909,348) or Gueguen et al (FR 2758626) or Bauer et al (DE 19813644 A1)

which describe the testing of circuits that use switching devices to control the application of voltage or current to various elements of the circuit.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward R. Cosimano whose telephone number is 571-272-0571. The examiner can normally be reached on 571-272-0571 from 7:30am to 4:00pm (Eastern time).

9.1 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow, can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9.2 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ERC
03/03/2007

Edward Cosimano

Edward Cosimano
Primary Examiner